Low-Loss Air-Isolated Through-Silicon Vias for Silicon Interposers

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***Abstract*—An air-isolated through-silicon via (TSV) technique is proposed to reduce radio-frequency (RF) losses in silicon interposers. A testbed containing air-isolated and conventional TSVs is fabricated and characterized from 10 MHz to 20 GHz with an L-2L de-embedding technique. The proposed air-isolated TSV technique yields 46.7% lower insertion loss compared to conventional TSVs at 20 GHz from 3-D full-wave simulations and measurements. Moreover, the impact of the air-isolation region width between TSVs on capacitance and conductance is quantified.**

***Index Terms*—Air-isolation, low-loss, silicon interposer, through-silicon via (TSV), 2.5-dimensional IC (2.5D IC).**

I. Introduction

SILICON interposers with high-density interconnects have been widely explored to obtain high-bandwidth chip-to-chip communication [1]. Moreover, silicon interposers enable the integration of heterogeneous technologies such as logic, radio-frequency microelectromechanical systems (RF MEMS), and passives yielding compact high-performance systems [2], [3]. However, the integration of these components necessitates large and thick silicon interposers to address warpage challenges [4], [5]. These thick interposers, in turn, result in increased TSV loss as well as capacitance and coupling between TSVs [6]. To address these challenges, various approaches have been demonstrated in the literature: low-k materials for the TSV liner or increased thickness of the TSV liner [7], high-resistivity silicon or glass substrates [7], [8], TSVs in polymer wells [9], coaxial TSVs [8], and an air-gap liner between a copper via and a silicon substrate [5]. Among the various approaches explored in the literature, obtaining an air-gap liner between the copper via and the silicon substrate has been of significant interest since the ε_r of air is approximately 1, which can significantly reduce the TSV capacitance and loss. Air-gap TSVs with improved electrical performance have been shown in the literature using sacrificial materials (e.g., poly propylene carbonate) or using silicon trench formation to achieve air liners [5], [10], [11]. However, due to wider air-gap liners, the fabrication of re-distribution layers (RDL) becomes difficult.

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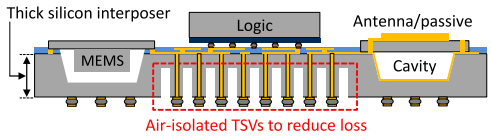

Fig. 1. Envisioned thick silicon interposer featuring air-isolated TSVs and supporting the integration of heterogeneous technologies such as RF MEMS and an antenna with a logic die in the interposer.

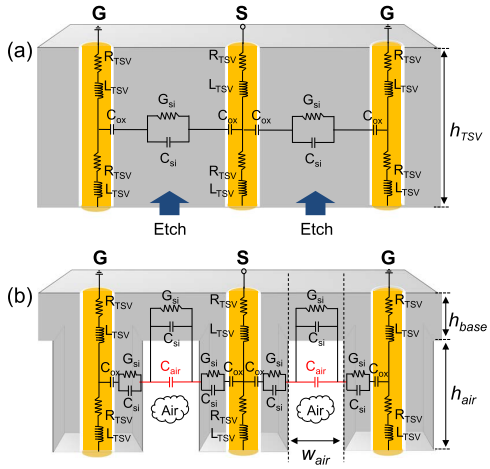

Fig. 2. Lumped circuit models of (a) conventional and (b) air-isolated TSVs.

To address these challenges, this letter introduces air-isolated TSVs for an envisioned thick silicon interposer supporting heterogeneous technologies, as shown in Fig. 1. The proposed TSVs are fabricated by etching silicon around each of the TSVs using the Bosch process to partially isolate them by air. This approach results in reduced RF losses, while enabling single-side metallization for RDL [4]. To extract the loss of a single TSV from a TSV-trace-TSV structure, a testbed of air-isolated TSVs with L-2L de-embedding [12] structures is presented. Lastly, the insertion loss of the air-isolated TSVs is compared to conventional TSVs of the same copper via dimensions, and the impact of air-isolation region width between TSVs on the capacitance and the conductance of TSVs is quantified.

II. Design of Air-Isolated TSVs With the L-2L De-Embedding Technique

Fig. 2 illustrates schematics of conventional and air-isolated TSVs along with their lumped circuit models [7]. In the model, the substrate portion of the air-isolated TSVs differs from

TABLE I
DIMENSIONS OF THE TSVS, THE SILICON PILLARS, AND THE METAL TRACES*

TSVs			Metal traces		Silicon pillars		
Radius	Height	Pitch	Top	Bottom	Width × Length	Height	w_{air}**
6.5	330	100/ 200	50 x 20	100 × 20 200 × 20	50 × 140 (L') 50 × 240 (2L')	230	50/100 /150

*All units are in microns.
**w_{air} refers to an air-isolation region width between silicon pillars. The widths of 100 μm and 150 μm are used only for a TSV pitch of 200 μm.

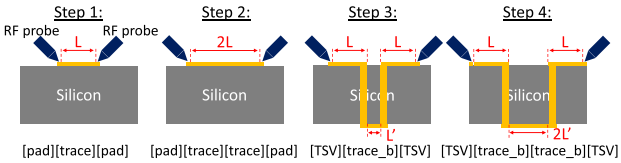

Fig. 3. L-2L de-embedding technique containing four measurement steps for extracting the loss of a single TSV, or [TSV], from a trace-TSV-trace structure.

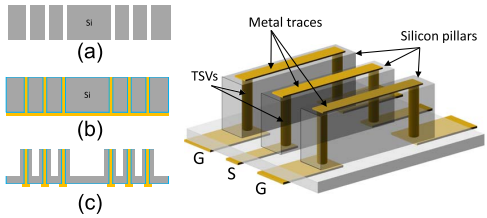

Fig. 4. Overall fabrication process flow of air-isolated TSVs (left) and a 3-D schematic of the proposed air-isolated TSVs for L-2L de-embedding (right).

conventional TSVs since there is an air region in parallel to a silicon base region, which partially isolates signal and nearby ground TSVs. This etched silicon region reduces TSV loss due to the reduced capacitance and conductance between TSVs. Table I summarizes the dimensions of the TSVs, the silicon pillars, and the metal traces. Moreover, the L-2L de-embedding technique is applied to extract the loss of a TSV from the structure of TSVs and metal traces, as illustrated in Fig. 3.

III. FABRICATION OF AIR-ISOLATED TSVS

Fig. 4 summarizes the fabrication process for the air-isolated TSVs. The fabrication begins with the deposition of silicon dioxide followed by an anisotropic oxide etch. Using the etched oxide as a hard mask, the Bosch process is used to etch through the silicon wafer [Fig. 4(a)]. In this process, the Bosch etching is utilized to fabricate highly scaled TSVs with an aspect ratio of 23 : 1 in a thick silicon substrate (∼330 μm thick). Following the Bosch process, thermal oxidation is performed to form a dielectric liner for the TSVs. To form a metal seed layer, titanium and copper are deposited using an e-beam evaporator at the back side of the wafer. The etched holes are filled with copper using bottom-up electroplating from the seed layer [Fig. 4(b)]. After electroplating, chemical mechanical polishing (CMP) is performed to remove over-electroplated copper, yielding 330 μm tall TSVs with 13 μm diameter. To facilitate probing, metal pads and traces are selectively deposited on TSVs at both sides of the wafer. Lastly, the Bosch process is performed from the back side of the wafer to attain the air-isolated TSV structure [Fig. 4(c)]. In this step, two lengths (L′ and 2L′) of

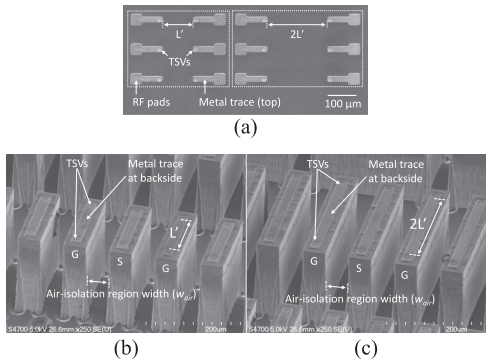

Fig. 5. SEM images of air-isolated TSVs; (a) illustrates RF pads and metal traces with TSVs from the top side; (b) and (c) show etched silicon pillars with TSVs and back metal traces of lengths of L' and 2L,' respectively.

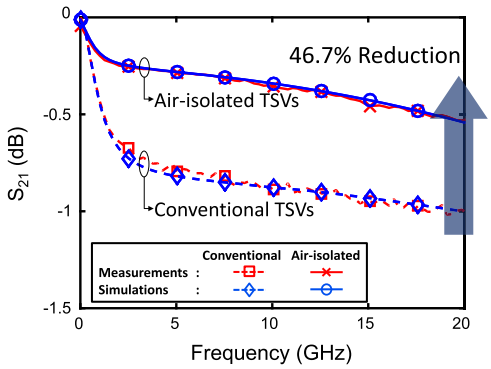

Fig. 6. Insertion loss (S21) comparison of conventional and air-isolated TSVs from measurements and simulations.

rectangular silicon pillars are fabricated for L-2L de-embedding [12], as shown in Fig. 5.

IV. HIGH-FREQUENCY CHARACTERIZATION WITH PROPOSED DE-EMBEDDING AND RESULTS

The fabricated testbed containing conventional and air-isolated TSVs is characterized using a microprobe station and an Agilent network analyzer. Using the de-embedding technique, the insertion loss of ground-signal-ground (GSG) TSVs is extracted from the measurements and the 3-D full-wave simulations, as shown in Fig. 6. The results show a 46.7% reduction in the insertion loss using the proposed air-isolated TSV technique at 20 GHz compared to conventional TSVs. Moreover, to analyze the reduction of TSV capacitance and conductance, single-port characterization is performed. Following S-parameter to Y-parameter conversion, the capacitance and the conductance of TSVs are extracted as

$$C_{\text{extracted}} = \frac{\text{Im}\,(Y_{11})}{\omega} \tag{1}$$

$$G_{\text{extracted}} = \text{Re}\,(Y_{11}) \tag{2}$$

where ω is an angular frequency [13]. To analyze the reduction in capacitance and conductance as a function of the width of the air-isolation region, three sets of air-isolated TSVs with air region widths of 50, 100, and 150 μm at a fixed TSV pitch of

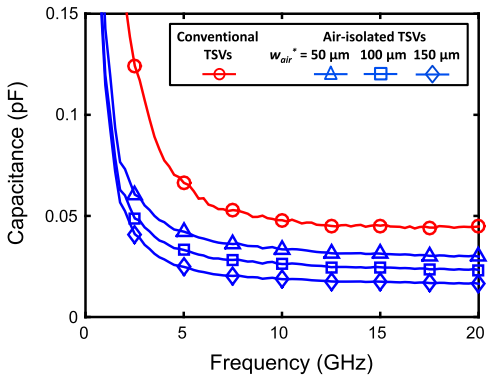

Fig. 7. Extracted capacitance from measurements: conventional and air-isolated TSVs with three air-isolation region widths.

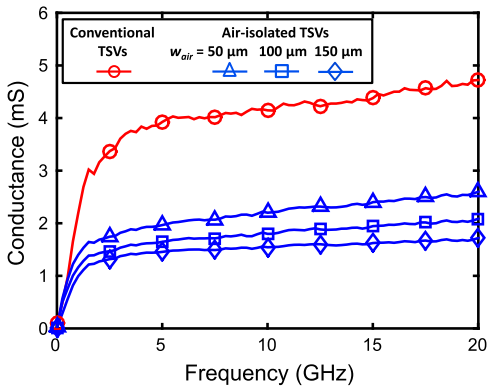

Fig. 8. Extracted conductance from measurements: conventional and air-isolated TSVs with three air-isolation widths.

TABLE II
EXTRACTED CAPACITANCE AND CONDUCTANCE FROM MEASUREMENTS: CONVENTIONAL AND AIR-ISOLATED TSVS WITH THREE AIR-ISOLATION REGION WIDTHS AT 20 GHZ (TSV PITCH OF 200 μm)

TSV Type	Conventional TSVs	Air-isolated TSVs		
		w_{air} = 50 μm	w_{air} = 100 μm	w_{air} = 150 μm
Capacitance	44.76 fF	29.90 fF	23.29 fF	16.46 fF
Reduction	N/A	33.2 %	48.0 %	63.2 %
Conductance	4.72 mS	2.60 mS	2.09 mS	1.72 mS
Reduction	N/A	44.9 %	55.7 %	63.6 %

*w_{air}: air-isolation region width

200 μm are characterized. It is observed that as the width of air increases between TSVs (for fixed TSV pitch), or equivalently the amount of silicon volume decreases, the capacitance and the conductance of TSVs reduces, as shown in Figs. 7 and 8. The results show that the capacitance of air-isolated TSVs decreases by 33.2%, 48.0%, and 63.2% compared to the capacitance of conventional TSVs at 20 GHz when the air-isolation region widths is 50, 100, and 150 μm, respectively. In similar manner, the conductance of air-isolated TSVs decreases by 44.9%, 55.7%, and 63.6%, respectively. The results are summarized in Table II. The reduction in loss and capacitance will enhance RF and digital signal transmission.

V. CONCLUSION

This letter proposes an air-isolated TSV technique for silicon interposers to reduce RF loss and capacitance. A testbed of conventional and air-isolated TSVs with L-2L de-embedding structures was fabricated and characterized from 10 MHz to 20 GHz. The measured results show that air-isolated TSVs reduce insertion loss by 46.7% compared to conventional TSVs of the same copper via dimensions at 20 GHz. Moreover, the capacitance and the conductance of TSVs decrease as the air-isolation region width increases, showing a maximum capacitance and conduction reduction of 63.2% and 63.6%, respectively, for an air-isolation region width of 150 μm at 20 GHz.

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